REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-4 and 6-27 remain in the application. Claims 1 and 27 have been amended. Claims 5 and 28 have been previously cancelled.

In item 1 on page 2 of the above-identified Office action, the drawings have been objected to under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims.

More specifically, the Examiner has stated that the read and write timing must be shown or the feature(s) cancelled from the claim(s). The features of read and write timing have been deleted from claim 27.

In item 3 on pages 3-4 of the above-mentioned Office action, claim 1 has been rejected as being anticipated by Applicants admitted prior art (AAPA) under 35 U.S.C. § 102(b).

In item 5 on pages 4-5 of the above-mentioned Office action, claims 2-3 and 27 have been rejected as being unpatentable over AAPA in view of Hiller et al. (US 5,081,575) under 35 U.S.C. § 103(a).

In item 6 on pages 5-6 of the above-mentioned Office action, claims 4, 6-7, 9-11, 14-17, and 19-20 have been rejected as being unpatentable over AAPA in view of Hiller et al. and further in view of Khandekar et al. (US 6,173,354) under 35 U.S.C. § 103(a).

In item 7 on pages 6-7 of the above-mentioned Office action, claims 8, 12-13, 18, 21-26 have been rejected as being unpatentable over AAPA in view of Hiller et al. and Khandekar et al. and further in view of Hanawa et al. (US 5,375,215) under 35 U.S.C. § 103(a).

The rejections have been noted and claims 1 and 27 have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in Fig. 1 and the corresponding description in the specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a first multiplexer associated with each of said at least one first device, each first multiplexer having <u>input connections connecting directly or via a pipeline stage</u>

to all of said at least one second device through read data buses and an output connection connecting to the associated one of said at least one first device through a read data bus;

an arbiter associated with each of said at least one second device, each arbiter having input connections connecting directly or via a pipeline stage to all of said at least one first device through address buses and an output connection connecting to the associated one of said at least one second device through an address bus; and

a second multiplexer associated with each of said at least one second device, each second multiplexer having input connections connecting directly or via a pipeline stage to all of said at least one first device through write data buses and an output connection connecting to the associated one of said at least one second device through a write data bus.

Claim 27 calls for, inter alia:

associating a first multiplexer with each of the at least one first device, each first multiplexer having input connections connecting directly or via a pipeline stage to all of the at least one second device through read data buses and an output connection connecting to the associated one of the at least one first device through a read data bus;

associating an arbiter with each of the at least one second device, each arbiter having input connections connecting directly or via a pipeline stage to all of the at least one first device through address buses and an output connection connecting to the associated one of the at least one second device through an address bus;

associating a second multiplexer with each of the at least one second device, each second multiplexer having input connections connecting directly or via a pipeline stage to all of the at least one first device through write data buses and an output connection connecting to the associated one of the at least one second device through a write data bus.

The language of claims 1 and 27 of the instant application has been modified to clearly recite the differences between the configuration according to the invention of the instant application as shown in Fig. 1 and the prior art configuration as shown in Fig. 2. More specifically, claims 1 and 27 now clearly recite that the first multiplexer (MUX1) associated with each first device (M1) has input connections connected directly or via a pipeline stage to all the second devices (S1, S2) through read data buses (READ2, READ3) and an output connection connecting to the associated first device through a read data bus (READ1); the arbiter (A1, A2) associated with each second device (S1, S2) has input connections connecting directly or via a pipeline stage to all the first devices through address buses (ADDR1) and an output connection connecting to the associated second device through an address bus (ADDR2, ADDR3); and the second multiplexer (MUX2, MUX3) associated with each second device has input connections connecting directly or via a pipeline stage to all first devices through write data buses (WRITE1) and an output connection connecting to the associated second device through a write data bus (WRITE2, WRITE3).

In contrast to the configuration as shown in Fig. 1, in the configuration as shown in Fig. 2 the input connections of the multiplexer (MUX11, MUX12, MUX13) associated with each first

device (M11, M12, M13) are connected to the second devices through the arbiter (A11, A12, A13) and the input connections of the arbiter (A11, A12, A13) associated with each second device (S11, S12, S13) are connected to the first devices through the multiplexer (MUX11, MUX12, MUX13). Further, since the arbiters (A1, A2) are connected to a respective one of the second devices through an address bus and the second multiplexers (MUX2, MUX3) associated with the second devices are connected to a respective one of the second devices through a write data bus, the arbiters and the second multiplexers associated with the second devices are separate devices. This contradicts the configuration as shown in Fig. 2 in which the Examiner has considered A11, A12, A13 as both an arbiter and a multiplexer.

The other cited references do not make up for the above deficiencies of the configuration as shown in Fig. 2.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 and 27. Claims 1 and 27 are, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-4 and 6-27 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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For Applicants

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